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## SMS DSP 10/100 100B-TX ETHERNET PHY

### OVERVIEW

SMS 10/100 ETHERNET PHY performs IEEE 802 10Base-T and 100Base-TX functionality as illustrated in Block diagram. It contains a completely integrated 100Base-Tx and 10Base-T PHYs with on chip transmit and receive filter functionality. MAC interface is through 10/100 basic MII interface as defined by 802.3 specifications (RMII and SMII options available). The mode of operation is selected through an external pin OR THROUGH AUTO NEGOTIATION LOGIC (COMPLIANT TO IEEE 802.3U STANDARD). Also, basic MII management interface (compliant to IEEE 802.3u standard) is included with basic register set defined in the standard. SMS PHY MII management registers set and programmability is compatible with both Level1 and National 10/100 PHY chips. An additional 5-bit symbol mode interface can be selected for use with repeater applications.

### 100BASE-TX MAIN FEATURES:

- Fully Integrated 100 Mb/s Cat-5 UTP Ethernet PHY Cell
- Complete On Chip 100Base-Tx / Cat-5 Solution Includes: Adaptive Equalizer, Data Recovery, scrambler, 4b/5b encoder, transmit PLL, mlt-3 transmit driver, supports 100Base-T MII.
- Complies with IEEE 802.3u 100Base-TX PHY specification.
- On chip advance DSP based adaptive equalizer: compensates for gain and phase distortion of any length of CAT-5 cable up to 160 meters. Also incorporates BASELINE wander correction capability.
- Superior DSP based CLOCK RECOVERY architecture.
- SYMBOL MODE cypher scrambler and descrambler for the reduction of EMI (TP-PMD standard ) are integrated.
- Output spectrum and strict rise & fall time control through waveform synthesis and current source output driver greatly reduces radiated emissions and eliminates EMI problems.
- 4b/5b encoding / decoding performed on unscrambled data for TP-PMD compatibility
- Supports SMII, RMII and media independent interface standards for controller interface;

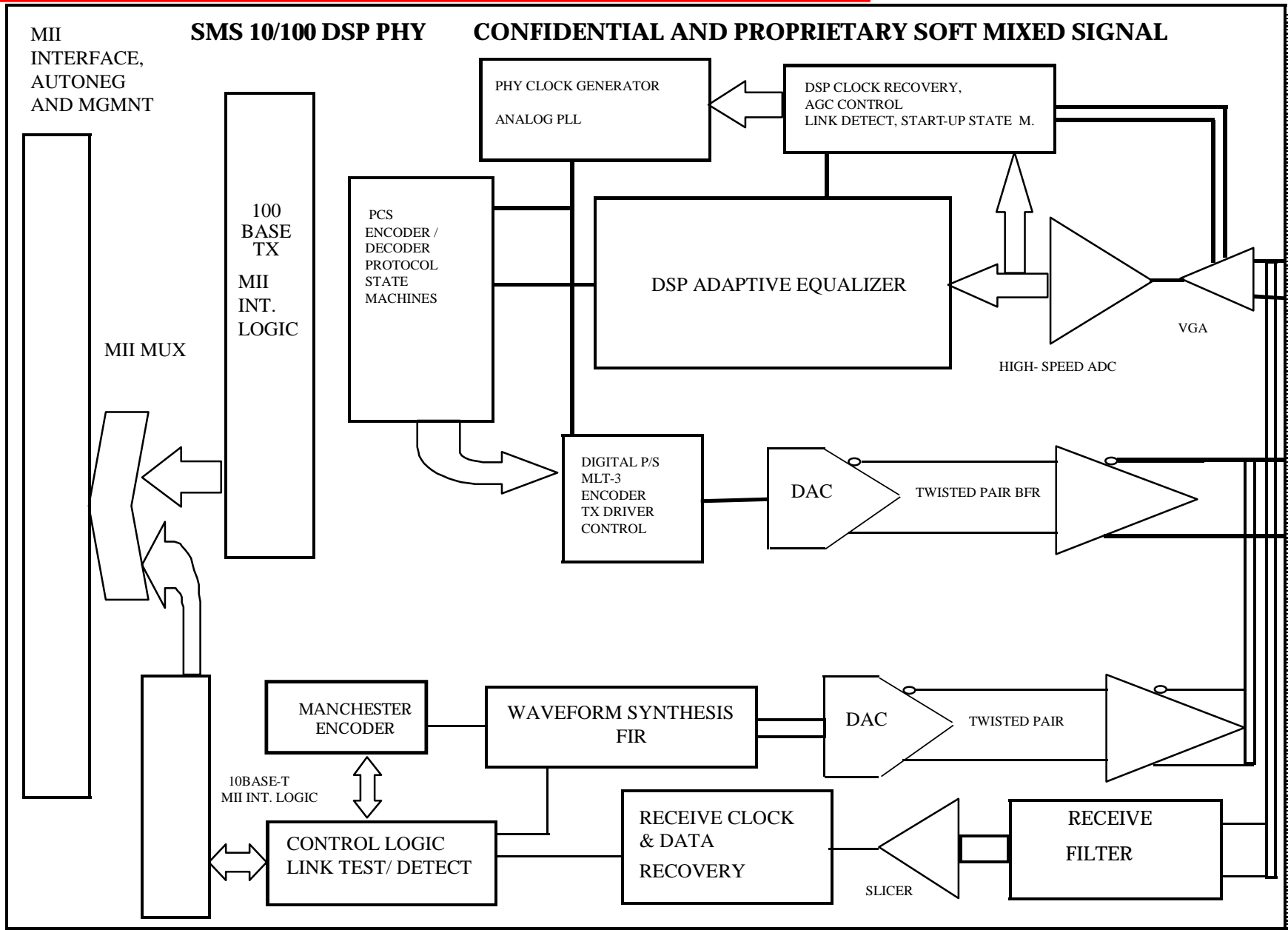
### 10BASE-T MAIN FEATURES:

The design essentially performs the IEEE 802.3 10BASE-T specification PMD / Transceiver function with necessary augments for FULL DUPLEX capability, which is currently an approved standard by IEEE 802.3 work-group. It functions as the interface between the filter and the transformer circuitry connected to the UTP and MEDIA INDEPENDENT INTERFACE connected to the IEEE 802.3 MAC (Media Access Control) Layer.

It contains all the necessary receive functions: Receive filter and slicer, polarity detect and correction, receive clock recovery and Manchester decoding. It performs Link test and detect functions and optionally collision detection. The transmit path, also, provides required Manchester Encoding, Transmit Clock Generation PLL circuits, By employing a proprietary FIR architecture performs Transmit wave-shaping, and high performance output buffer to directly drive the UTP transformer and necessary bias and reference generation circuits.

- Reduction in total system cost: Both transmit and receive filters are integrated on chip
- Complies with IEEE 802.3 10base-T Specification and Full Duplex capable
- Independent clock recovery for each transceiver.
- MAC interface through IEEE 802.3 MII functionality.
- Output spectrum and strict harmonic control through wave-form synthesis and high performance output driver greatly reduces radiated emissions and eliminates EMI problems.

- LINK TEST / DETECT and optional collision logic supported.



## **SEAMLESS SEMICONDUCTOR IP CORE IMPLEMENTATION**

- **Digital DSP based Architecture**
- **Complete System Simulation Platform provided; Verilog and Mixed Signal Extensions**

**To Verilog enable simulation and testing of complete system for System On chip Implementations**

- **Extensive testability and Diagnosis capability incorporated**
- **Design Flow and methodology enables use of state-of-the-art, standard IC design**

**Methodology including Synthesis, Simulation, Place and Route tools.**