SMS2012 — *SONET/SDH OC-12 TRANSCEIVER/ CDR*

FEATURES

- Innovative (patent pending) CMOS architecture to guarantee compliance with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer, and jitter generation
- Designed for multiple integration in typical SOC applications
- High frequency PLLs with integrated on chip loop filters
- Advanced Signal Processing techniques utilized for clock recovery
- Supports 622.08 Mbit/s (OC-12)
- Selectable reference frequencies of 77.76 or 155.52 MHz
- LVPECL or LVDS logic for external interfacing to optical units
- Diagnostic Loopback mode

APPLICATIONS

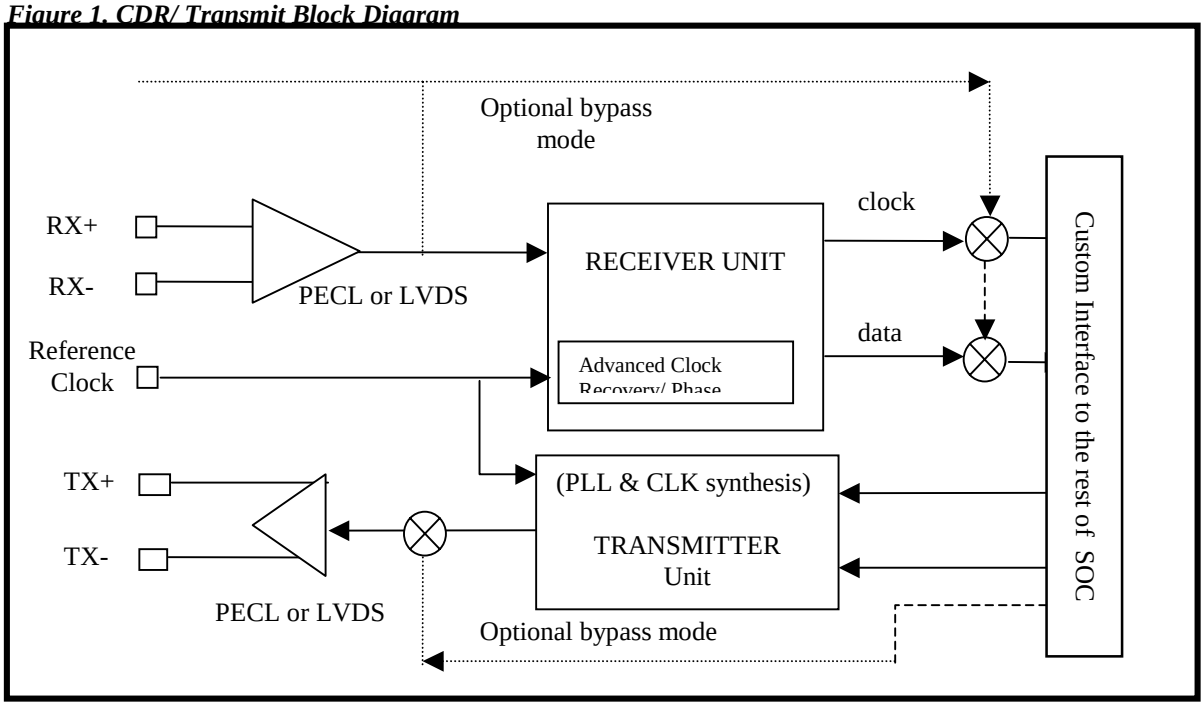
- SONET/SDH-based transmission systems
- WDM/ DWDM aggregator ICs
- SONET/SDH modules
- SONET/SDH test equipment
- Packet Over SONET (POS)
- ATM over SONET
- IP over SONET
- Add Drop Multiplexer (ADM)
- Broad-band cross-connects

GENERAL DESCRIPTION

The SMS2012 SONET/SDH is a fully integrated Clock Data Recovery (CDR) SONET OC-3 interface core designed for multiple integration on a single IC in a typical System-On-Chip (SOC) application. SMS2012 interfacing to the rest of building blocks on chip is fully customizable. For example, an optional mux-demux module can be interconnected to the SMS2012 core making it capable of performing all the necessary serial-to-parallel and parallel-to-serial functions in compliance with SONET/SDH transmission standards. The SMS2012 block diagram is shown in Figure 1. In a typical SOC application, 16 instances of SMS2011 (SONET/SDH OC-3 TRANSCEIVER / CDR), 4 instances of SMS2012 and an additional 2 million of logic gates can be integrated on a single chip.

SMS2012 CDR block contains a *clock recovery unit* with an *integrated loop filter* allowing the use of a slower clock reference. SMS2012 performs the clock recovery task by utilizing proprietary Advanced Signal Processing techniques. The interface to an external optical module could be either LVPECL or LVDS. The low jitter LVPECL/ LVDS interface guarantees compliance with the bit-error rate requirements of the ITU standards.

Figure 1. CDR/ Transmit Block Diagram



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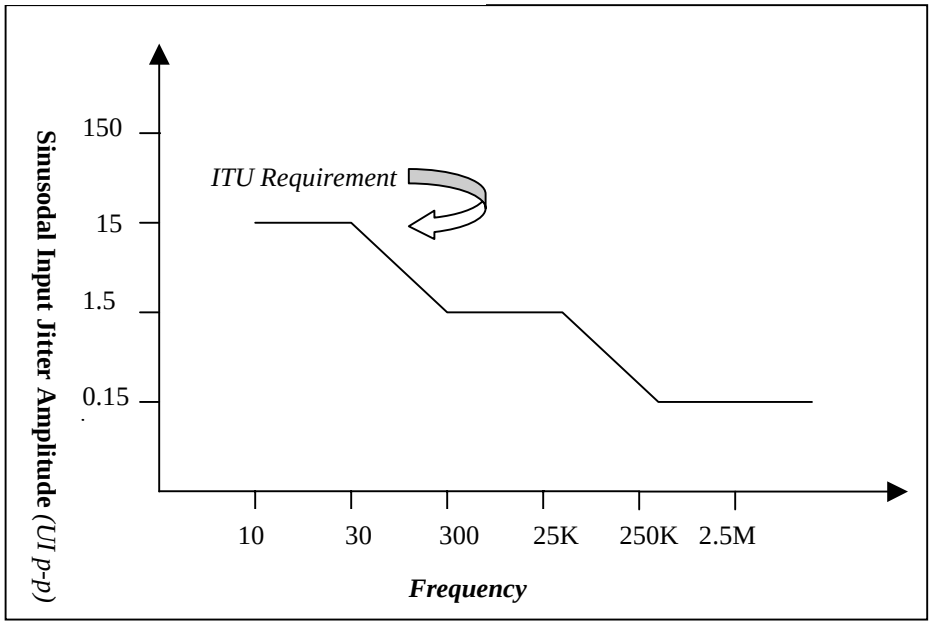
Functional Description

As shown in Figure 1, the SMS2012 is divided into the *receive section*, the *transmitter section,* and the *custom interface section*. The SMS2012 could serve as a building block of a highly integrated SONET/SDH SOC device and function as the primary physical interface between SONET/SDH optical equipment and the SONET/SDH framer implemented on the same silicon chip. The incoming reference clock frequency can be 77.76 or 155.52 MHz in support of existing system clocking schemes. The reference clock is required for the proper operation of the CDR architecture and to provide a stable output clock source in the absence of serial input data. The interface to optical module could be either LVPECL or LVDS. The low jitter LVPECL/ LVDS interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. An optional module could be added to de-serialize the incoming higher frequency data into a lower frequency if needed. In the transmit section, the SMS2012 transmits the output data of the optional serializer module utilizing its high clock synthesis module which also manages the jitter performance. The transmit section interface with an external optical module could be either LVPECL or LVDS to guaranteed compliance with Bellcore and ITU-T standards.

Jitter Performance

TheSMS2012 PLLs fully meets the jitter specifications (Input Jitter Tolerance and Jitter Transfer Requirement) proposed for SONET/SDH equipment as specified in ITU documents. The CDR unit uses an innovative (patent pending) architecture to comply with the SONET/SDH (Figure 2.). This jitter performance is achieved even in presence of the noise sources generated by high speed switching activities of other logical blocks in a typical SOC design environment.

Figure 2. Input Jitter Tolerance



Power Consumption

Utilizing a typical single poly 0.25 micron (drawn) CMOS process, the IDD current is limited to 20mA operating out of 3.3 Volt power supply in the IO region of a chip. This current consumption does not include the power consumed by the PECL or LVDS differential IO drivers.

SOC place & Route consideration

SMS2012 is implemented using a *modular hard macro* (fixed layout) methodology. However, to facilitate ease of integration in a typical SOC application, the aspect ratio of the SMS2012 layout core is variable. SMS2012 current core size implemented in a 4-layer metal 0.25 micron CMOS technology is 1.2 mm^2.

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